REMARKS

Claims 1-14, 16-20, and 23-25 were previously pending in this patent application. Claims 1-14, 16-20, and 23-25 stand rejected. Herein, Claims 1, 8, 20, and 23 have been amended to correct typographical errors. Accordingly, after this Amendment and Response After Final action, Claims 1-14, 16-20, and 23-25 remain pending in this patent application. Further examination and reconsideration in view of the claims, remarks, and arguments set forth below is respectfully requested.

35 U.S.C. Section 102(e) Rejections

Claims 1-14, 16-20, and 23-25 stand rejected under 35 U.S.C. 102(e) as being anticipated by Lee et al., U.S. Patent Application Publication No. US2003/0158995 (hereafter Lee). These rejections are respectfully traversed.

Independent Claim 1 recites (as amended):

> A variable width memory system comprising:
> a bus for communicating information;
> a plurality of ***variable width memory locations*** coupled to said bus, said plurality of ***variable width memory locations store information***, wherein said plurality of ***variable width memory locations receive a number of bits corresponding to the width of the variable width memory locations***; and
> a controller coupled to said bus, said controller directs access to said plurality of variable width memory locations, wherein said number of bits potentially vary automatically on a per access basis depending on which variable width memory location of said plurality of variable width memory locations is being accessed, wherein all memory locations are not required to have the same width. (emphasis added)

It is respectfully asserted that Lee does not disclose the present invention as recited in Independent Claim 1. In particular, Independent Claim 1 recites the limitations, "a plurality of ***variable width memory locations***," (emphasis added), "plurality of ***variable width memory locations store information***," (emphasis added), and "plurality of ***variable width memory locations receive a number of bits corresponding to the width of the variable***

width memory locations," (emphasis added). In contrast, Lee is directed to paging. [Lee; Abstract; paragraphs 0004 and 0020]. A page is defined as an area in a memory bank accessed by a given row address. Id. A page is "opened" when a given row address is strobed into the memory bank. Id. If a series of accesses are all to the same page, then once the page is open, only column addresses need to be strobed into the memory bank. Id. Thus the RAS (row address strobe) precharge time is saved for each subsequent access to the open page. Id. Therefore, paging involves leaving a memory page open as long as accesses continue to "hit" within that page. Id.

That is, Lee discloses a memory address scheme based on paging to improve memory throughput instead of disclosing variable width memory locations, as in the invention of Independent Claim 1. A page only refers to an area in a memory bank accessed by a given row address. The actual memory locations within the page are accessed with the given row address and appropriate column addresses, wherein the actual memory locations store information and receive bits to be stored. Lee does not disclose anything concerning variable width memory locations, information stored in variable width memory locations, and number of bits received by the variable width memory locations corresponding to the width of the variable width memory locations, as in the invention of Independent Claim 1.

Moreover, when Lee discusses adjustable page size, the discussion simply refers to a memory that has multiple memory modules and multiple memory types, wherein the memory type (generally denoted by BA x RA x CA, where RA is the number of row address bits, CA is the number of column address bits, and BA is the number of bank address bits) determines the maximum page size of a memory module by the formula: max. page size = 2^{CA} x 2^3. [Lee; paragraphs 0005 and 0006]. Thus, when a memory module is

selected, its corresponding maximum page size is utilized instead of all the memory modules using the same page size. [Lee; Figure 5; paragraphs 0021 through 0032]. As described above, a page refers to an area of a memory bank and is not an actual memory location since an actual memory location within the page is accessed with the given row address and an appropriate column address. Thus, an adjustable page size is not equivalent to a variable width memory location. Therefore, it is respectfully submitted that Independent Claim 1 is not anticipated by Lee and is in condition for allowance.

Dependent Claims 2-7 are dependent on allowable Independent Claim 1, which is allowable over Lee. Hence, it is respectfully submitted that Dependent Claims 2-7 are patentable over Lee for the reasons discussed above.

With respect to Independent Claims 8, 20, and 23, it is respectfully submitted that Independent Claims 8, 20, and 23 recite similar limitations as in Independent Claim 1. In particular, Independent Claim 8 recites the limitations, "***accessing a memory cell*** based on said register indicator, wherein said memory cell is ***allocated a storage size correlating to the bit capacity of said register***," (emphasis added) and, "***transferring information*** between said memory cell and another component, wherein said ***information includes the same number of bits as said bit capacity***", (emphasis added). The cited limitations are directed to accessing a memory cell that is allocated a storage size correlating to the bit capacity of a register, and are directed to transferring information that has the same number of bits as the bit capacity of the register between the memory cell and another component. That is, the storage size of the memory cell is variable since it is correlated to the bit capacity of a register. Further, Independent Claim 20 recites the limitation, "assigning ***a memory***

location a width equal to the number of said bits in said portion of said block of data", (emphasis added). That is, the width of a memory location is variable since it is equal to the number of bits in a portion of a block of data. Furthermore, Independent Claim 23 recites the limitation, "a means for ***storing information*** in ***uniquely identifiable different width memory locations*** corresponding to said memory location identifiers," (emphasis added). Lee does not disclose the cited limitations of the inventions of Independent Claims 8, 20, and 23. Therefore, Independent Claims 8, 20, and 23 are not anticipated by Lee and are allowable for reasons discussed in connection with Independent Claim 1.

Dependent Claims 9-14, Dependent Claims 16-19, and Dependent Claims 24-25 are dependent on allowable Independent Claims 8, 20, and 23 respectively, which are allowable over Lee. Hence, it is respectfully submitted that Dependent Claims 9-14, Dependent Claims 16-19, and Dependent Claims 24-25 are patentable over Lee for the reasons discussed above.

CONCLUSION

It is respectfully submitted that the above claims, arguments, and remarks overcome all rejections. All remaining claims (Claims 1-14, 16-20, and 23-25) are neither anticipated nor obvious in view of the cited references. For at least the above-presented reasons, it is respectfully submitted that all remaining claims (Claims 1-14, 16-20, and 23-25) are in condition for allowance.

The Examiner is urged to contact Applicant's undersigned representative if the Examiner believes such action would expedite resolution of the present Application.

Please charge any additional fees or apply any credits to our PTO deposit account number: 23-0085.

Respectfully submitted,

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